We claim:

1. A reference signal generator, comprising:
an oscillator that provides an oscillator signal;
a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said amplifier gain in response to said reference amplitude.

2. The generator of claim 1, wherein said controller is configured to initiate said amplifier gain at a predetermined amplifier gain and subsequently adjust said amplifier gain to a controlled amplifier gain.

3. The generator of claim 2, wherein said predetermined amplifier gain is a maximum amplifier gain and said controller is configured to subsequently reduce said amplifier gain to said controlled amplifier gain.

4. The generator of claim 3, wherein said controller includes a comparator that stops reduction of said amplifer gain when said reference amplitude corresponds to a threshold amplitude.

5. The generator of claim 2, wherein said predetermined amplifier gain exceeds said controlled amplifier gain.

6. The generator of claim 2, wherein said controlled amplifier gain exceeds said predetermined amplifier gain.

7. The generator of claim 1, wherein said controller includes:
a clock that provides a clock signal;
a counter set to an initial count that maximizes said ampifier gain and coupled to provide a subsequent count of said clock signal that reduces said amplifer gain; and
a comparator that terminates said subsequent count in response

to said reference amplitude and a threshold amplitude.

8. The generator of claim 1, wherein said buffer amplifier includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.

9. The generator of claim 1, wherein said amplifier gain is less than one.

10. The generator of claim 1, wherein said oscillator is a digitally-controlled crystal oscillator.

11. A reference signal generator, comprising:

an oscillator that provides an oscillator signal;

a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and

a controller that adjusts said amplifier gain in response to said reference amplitude.

12. The generator of claim 11, wherein said buffer amplifier includes a plurality of current genrators that are responsive to said controller.

13. The generator of claim 12, wherein each of said current generators includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.

14. The generator of claim 11, wherein said buffer amplifier

provides said reference signal at a reference port and each of said current generators includes:

a plurality of resistors;

a plurality of access switches that access selected ones of said resistors in response to said controller; and

an output switch that couples selected resistors to said reference port in response to said oscillator signal.

15. The generator of claim 11, wherein said amplifier gain is responsive to a gain control signal and said controller includes a comparator that determines said gain control signal in response to said reference signal and a threshold signal.

16. The generator of claim 15, wherein said controller further includes:

a string of resistors coupled to provide selectable voltages; and

a plurality of transistors coupled to selectively provide one of said voltages as said threshold signal.

17. The generator of claim 15, wherein said comparator comprises a differential pair of transistors that determines said gain control signal in response to said reference signal and said threshold signal.

18. The generator of claim 11, wherein said amplifier gain is responsive to a digital gain control signal and said controller includes:

a clock that provides a clock signal;

a counter that counts said clock signal to thereby generate said digital gain control signal; and

a comparator that passes said clock signal to said counter in response to a comparison of said reference signal and a threshold signal.

19. The generator of claim 18, wherein said clock includes at least one divider that divides said oscillator signal to thereby generate

said clock signal.

20. The generator of claim 11, wherein:
said buffer amplifier includes:
a) a plurality of resistors; and
b) a plurality of switches that selectively access said resistors in response to a gain control signal;
and said controller includes a comparator that provides said gain control signal in response to said reference signal and a threshold signal.

21. The generator of claim 20, wherein said comparator comprises a differential pair of transistors that determines said gain control signal in response to said reference signal and said threshold signal.

22. The generator of claim 18, wherein said controller includes:
a clock that provides a clock signal;
a counter that counts said clock signal to thereby generate said gain control signal; and
a comparator that passes said clock signal to said counter in response to a comparison of said reference signal and a threshold signal.

23. The generator of claim 22, wherein:
said controller is configured to initially reset said counter to thereby provide an initial version of said gain control signal that maximizes said amplifier gain; and
said counter counts said clock signal to cause said gain control signal to reduce said amplifier gain.

24. The generator of claim 11, wherein said amplifier gain is less than one.

25. The generator of claim 11, wherein said oscillator is a

digitally-controlled crystal oscillator.

26. A synthesizer, comprising:
a voltage-controlled oscillator;
a phase detector that provides a control signal to said voltage-controlled oscillator;
a first frequency divider coupled between said voltage-controlled oscillator and said phase detector;
an oscillator that generates an oscillator signal;
a second frequency divider coupled between said reference oscillator and said phase detector;
a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said amplifier gain in response to aid reference amplitude.

27. The synthesizer of claim 26, wherein said controller is configured to:
initiate said amplifier gain at a maximum amplifier gain; and
subsequently reduce said amplifier gain to a controlled amplifier gain.

28. The synthesizer of claim 26, wherein said controller includes a comparator that stops reduction of said amplifer gain when said reference amplitude corresponds to a threshold amplitude.

29. The synthesizer of claim 26, wherein said controller includes:
a clock that provides a clock signal;
a counter set to an initial count that maximizes said amplifier gain and coupled to provide a subsequent count of said clock signal that reduces said amplifier gain; and
a comparator that terminates said subsequent count in response to said reference amplitude and a threshold amplitude.

30. The synthesizer of claim 26, wherein said buffer amplifier includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.